SAHRDAYA COLLEGE OF ENGINEERING AND TECHNOLOGY, KODAKARA - 680684

BRANCH: ELECTRONICS AND COMMUNICATION ENGINEERING **SEMESTER: S7**

Room No. 101 (Bio Block) **CLASS TIME TABLE** **With effect from: 10-09-2023**

Day	09:00 - 09:50 AM	09:50 - 10:45 AM	10.45-11.00 AM	11:00 – 12 NOON	12.00 - 12:45 PM	12:45 - 1:30 PM	01:30 - 02:20 PM	02:20 - 02:35 PM	02.35-03.30 PM	03:30 - 04:20 PM
Mon	OFC (Dr.Vishnu)	M&A (Chinchu)	Break	OFC/M&A(T) (Dr.Vishnu /Chinchu)	Lunch	Open Elective		Break	ISE (Ambily)	OFC (Dr. Vishnu)
Tue	M&A (Chinchu)	ISE (Ambily)		M&A/OFC(T) (Chinchu/Dr.Vishnu)		Open Elective			OFC (Dr. Vishnu)	ISE (Ambily)
Wed	Project Phase 1 (Dr.Vishnu/Minu)									
Thur	ISE (Ambily)	OFC (Dr.Vishnu)	Break	M&A (Chinchu)		Electromagnetics Lab(Chinchu,Ambily):Batch A Seminar (Binet Rose,Dr.King) :Batch B				
Fri	OFC (Dr.Vishnu)	M&A (Chinchu)		Placement Training		Electromagnetics Lab(Chinchu,Ambily):Batch B Seminar (Binet Rose,Dr.King) :Batch A				
Sat	Special Timetable									

Course Name	Course Code	Course name	Name of Faculty	
M&A (4+1)	:ECT 401	Microwaves and Antenna	(Ms.Chinchu Jose)	A Batch: Roll Nos:1-28
OFC(5+1)	:ECT 413	Optical Fiber Communication	(Dr.Vishnu Rajan)	B Batch: Roll Nos:29-56
O/E(4)	:ECT 415	Mechatronics	(Dr.Silpa P.A.)	
ISE (4 +1)	:MCN 401	Industrial Safety Engineering	(Ms.Ambily Francis)	
EML(8)	:ECL 411	Electromagnetics Lab	(Ms.Chinchu Jose,Ms.Ambily Francis)	
S(8)	:ECQ 413	Seminar	(Ms.Binet Rose Devassy, Dr.Gnana King)	
PP(6)	:ECD 415	Project Phase 1	(Dr. Vishnu Rajan, Ms.Minu Johny)	
PT		Placement Training		
Minor/R	:ECD 481	Miniproject	(Dr. Vishnu Rajan)	

Total Hours (35)

Prepared by: Chinchu Jose **Verified by: HOD** **Approved by: Principal**

SAHRDAYA COLLEGE OF ENGINEERING AND TECHNOLOGY, KODAKARA - 680684

BRANCH: ELECTRONICS AND COMMUNICATION ENGINEERING **SEMESTER: 5**

Room No. 108 (Bio Block) **CLASS TIME TABLE** **With effect from: 03-08-23**

Day	09:00 - 09:50 AM	09:50 - 10:45 AM	10.45-11.00 AM	11:00 – 12 NOON	12.00 - 12:45 PM	12:45 - 1:30 PM	01:30 - 02:20 PM	02:20 - 02:35 PM	02.35-03.30 PM	03:30 - 04:20 PM
Mon	LIC (Binet)	CS (Ambily)	Break	DSP/LIC(T) (Dr.King/Binet)		AIC LAB (Naiji, Binet Rose):Batch A DSP Lab (Dr.King,Vidyamol):Batch B				
Tue	DSP (Dr.King)	LIC (Binet)		DM (Vidyamol)		AIC LAB (Naiji, Binet Rose):Batch B DSP Lab (Dr.King,Vidyamol):Batch A				
Wed	ADC (Minu)	DSP (Dr.King)		ADC/CS(T) (Minu/Ambily)		IEFT (Vini)	DSP (Dr.King)	Break	LIC (Binet)	CS (Ambily)
Thur	DM (Vidyamol)	LIC (Binet)		CS/ADC(T) (Ambily/Minu)		ADC (Minu)	IEFT (Vini)		IEFT (Vini)	ADC (Minu)
Fri	CS (Ambily)	DSP (Dr.King)		CS (Ambily)		LIC /DSP (T) (Binet/Dr.King)	DM (Vidyamol)		SGA	ADC (Minu)
Sat	Special Timetable									

Course Name	Course Code	Course name
LIC(4+1)	:ECT 301	Linear Integrated Circuits
DSP(4+1)	:ECT 303	Digital Signal Processing
ADC (4+1)	:ECT 305	Analog And Digital Communication
CS(4+1)	:ECT 307	Control System
IEFT(3)	:HUT 300	Industrial Economics and Foreign Trade
DM(3)	:MCN 301	Disaster Management
AICL(4)	:ECL 331	Analog Integrated Circuits And Simulation Lab
DSPL(4)	:ECL 333	Digital Signal Processing Lab
SGA(1)		Study Group Activity

Name of Faculty	
(Ms.Binet Rose Devassy)	A Batch: Roll Nos:1-31
(Dr. Gnana King)	B Batch: Roll Nos:32-62
(Ms. Minu C Davis)	*Total Hours (35)*
(Ms. Ambily Francis)	
(Ms.Vini Valsan)	
(Ms.Vidyamol)	
(Ms.Naiji Joseph, Ms.Binet Rose Devassy)	
(Dr. Gnana King, Ms.Vidyamol)	
(Ms.Anju Babu, Dr.Gnana King, Ms.Ambily Francis)	

Prepared by: Chinchu Jose **Verified by: HOD** **Approved by: Principal**

SAHRDAYA COLLEGE OF ENGINEERING AND TECHNOLOGY, KODAKARA - 680684

BRANCH: ELECTRONICS AND COMMUNICATION ENGINEERING **SEMESTER: S3**

Room No. 003 (Bio Block) **CLASS TIME TABLE** **With effect from:04-09-2023**

Day	09:00 - 09:50 AM	09:50 - 10:45 AM	10.45-11.00 AM	11:00 – 12 NOON	12.00 - 12:45 PM	12:45 - 1:30 PM	01:30 - 02:20 PM	02:20 - 02:35 PM	02.35-03.30 PM	03:30 - 04:20 PM
Mon	PDCA (Anu)	LCD (Vidyamol)		NT (Naiji)		SSD (Dr.Arun)	SE (Chinchu)		PDCA (Anu)	DE (Minu)
Tue	LCD (Vidyamol)	NT (Naiji)		SSD (Dr.Arun)		SE (Chinchu)	PDCA (Anu)		DE (Minu)	SSD/PDCA(T) (Dr.Arun/Anu)
Wed	SSD (Dr.Arun)	NT (Naiji)		SE (Chinchu)		Scientific Computing Lab(Minu,Dr.Arun):Batch A Logic Design Lab (Viyamol,Dr.Silpa):Batch B				
Thur	NT (Naiji)	SSD (Dr.Arun)		LCD (Vidyamol)		Scientific Computing Lab(Minu,Dr.Arun):Batch B Logic Design Lab (Viyamol,Dr.Silpa):Batch A				
Fri	PDCA (Anu)	NT/LCD(T) (Naiji/Vidyamol)		PDCA/SSD(T) (Anu /Dr.Arun)		DE (Minu)	SSD (Dr.Arun)		SGA	LCD/NT(T) (Vidyamol/Naiji)
Sat	Special Timetable									

Course Name	Course Code	Course name
PDCA(3+1)	:MAT 201	Partial Differential Equation and Complex Analysis
SSD(4+1)	:ECT 201	Solid State Devices
LCD(3+1)	:ECT 203	Logic Circuit Design
NT(4+1)	:ECT 205	Network Theory
DE(3)	:EST 200	Design and Engineering
SE(3)	:MCN 201	Sustainable Engineering
SCL(3)	:ECL 201	Scientific Computing Lab
LDL(3)	: ECL 203	Logic Design Lab
R/M(4)	:VAC	
SGA(1)	: Study Group Activity	

Name of Faculty

(Ms. Anu Joseph)) A Batch: Roll Nos:1-32

(Dr.Arun K V) B Batch: Roll Nos:33-63

(Ms.Vidyamol) *Total Hours (35*

(Ms.Naiji Joseph)

(Ms.Minu Johny)

(Ms. Chinchu Jose)

(Ms.Minu Johny,Dr.Arun A V)

(Ms.Vidyamol K,Dr.Silpa P.A.)

(Dr.Arun A.V,Ms.Chinchu Jose,Dr.Silpa P.A.)

Prepared by: Chinchu Jose

Verified by: HOD

Approved by: Principal

SAHRDAYA COLLEGE OF ENGINEERING AND TECHNOLOGY, KODAKARA - 680684

BRANCH: ELECTRONICS AND COMMUNICATION ENGINEERING SEMESTER: S1 M Tech EMBEDDED SYTEM

Room No. 205 (KC) **CLASS TIME TABLE** **With effect from: 04/09/2023**

Day	09:00 - 09:50 AM	09:50 - 10:45 AM	10:45 - 11:00 AM	11:00 - 12:00 PM	12:00 - 12:45 PM	12:45 - 1:30 PM	01:30 - 02:20 PM	02:20 - 03:15 PM	03:15 - 03:30 PM	03:30 - 04:20 PM
Mon	EP (Dr.King)	SDEP (Dr. Arun)	Tea Break	AEM (Savitha)	Lunch break	EP Lab (Anju/Ambily)		TA/LR	Tea Break	TA/LR
Tue	AEM (Savitha)	TA/LR		EP (Dr.King)		CC (Anju)	SDEP (Dr. Arun)	TA/LR		TA/LR
Wed	STM (Binet)	CC (Anju)		AEM (Savitha)		STM (Binet)	TA/LR	TA/LR		EP (Dr.King)
Thur	CC (Anju)	EP (Dr.King)		RM (Dr.Silpa)		TA/LR	TA/LR	TA/LR		TA/LR
Fri	SDEP (Dr. Arun)	AEM (Savitha)		STM (Binet)		RM (Dr.Silpa)	SDEP (Dr. Arun)	TA/LR		TA/LR
Sat	Special Timetable									

AEM(4)	: 221TEC100	:Advanced Engineering Mathematics	(Ms. Savitha Thomas)
SDEP(4)	: 221TEC001	: System Design using Embedded Processors	(Dr.Arun A V)
EP(4)	:221TEC002	: Embedded Programming	(Dr.Gnana King)
E-CC (3)	: 221EEC002	: Cloud Computing	(Ms.Anju Babu)
E-STM(3)	: 221EEC009	: Sensor Technologies and MEMS	(Ms.Binet Rose)
RM(2)	: 221RGE100	: Research Methodology	(Dr.Silpa P A)
EPL(2)	: 221LEC100	: Embedded Processors Laboratory	(MsAnju Babu /Ms..Ambily Francis)

Prepared by: Binet Rose **Verified by: HOD** **Approved by: Principal**